Transition-Mode PFC Controller ME8401

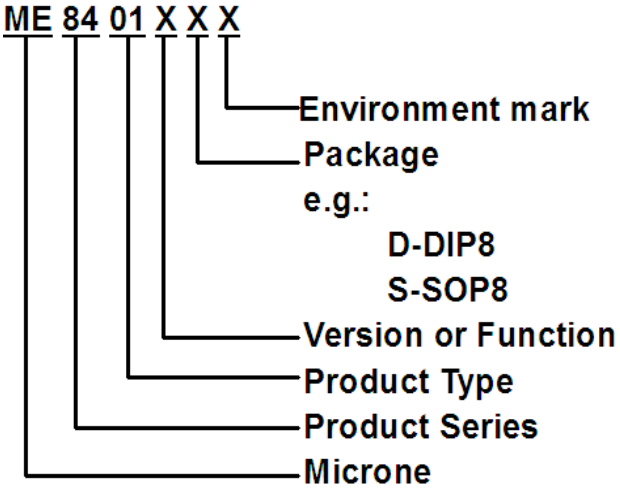
General Description

The ME8401 is a current-mode PFC controller operating in Transition Mode (TM). Pin-to-pin compatible with the predecessor ME8401, it offers improved performance.
The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range. The output voltage is controlled by means of a voltage-mode error amplifier and a precise (1% @Tj =25°C) internal voltage reference. The device features extremely low consumption (≤120 uA before start-up and <2mA running) and includes a disable function suitable for IC remote ON/OFF, which makes it easier to comply with energy saving norms (Blue Angel, EnergyStar, Energy2000, etc.). An effective two-step OVP enables to safely handle overvoltage either occurring at start-up or resulting from load disconnection. The totem-pole output stage, capable of 600mA source and 800mA sink current, is suitable for big MOS-FET or IGBT drive which, combined with the other features, makes the device an excellent low-cost solution for EN61000-3-2 compliant SMPS's up to 300W.

Features

- ●Transition-Mode control of PFC pre-regulators
- ●Proprietary multiplier design for minimum THD of AC input current
- ●Very precise adjustable output overvoltage protection
- ●Ultra-low(≤120uA) start-up current
- ●Extended IC supply voltage range
- ●On-chip filter on current sense
- ●Disable function
- ●1%(@ Tj = 25 °C) internal reference voltage
- ●-600/+800mA totempole gate driver with UVLO pull-down and voltage clamp
- ●DIP-8/SOP-8 packages

Selection Guide

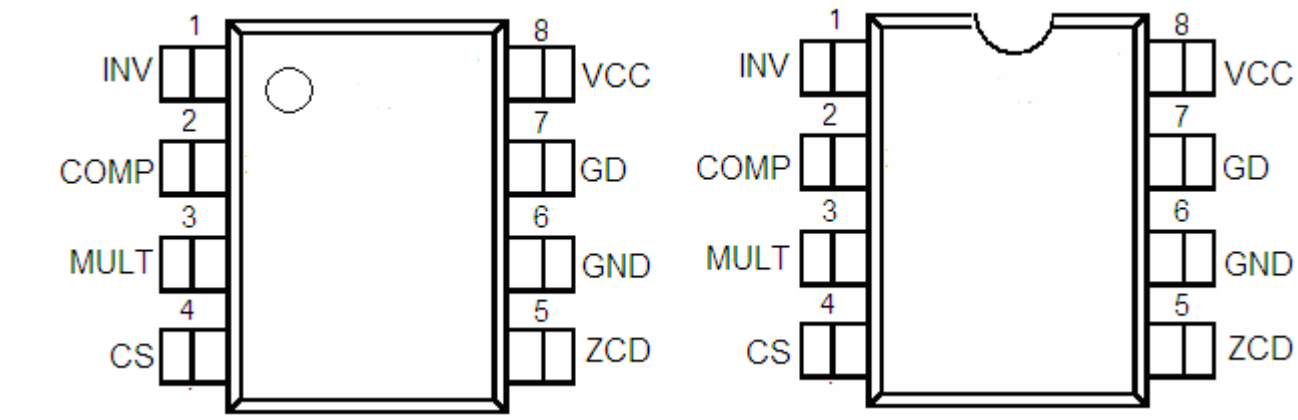


Applications

PFC pre-regulators for:

- ●IEC61000-3-2 compliant SMPS(TV, Desktop PC, Monitor) up to 300W
- ●Hi-end AC-DC adapter/charger
- ●Entry level server & web server

Pin Configuration (Top view)



Pin Assignment

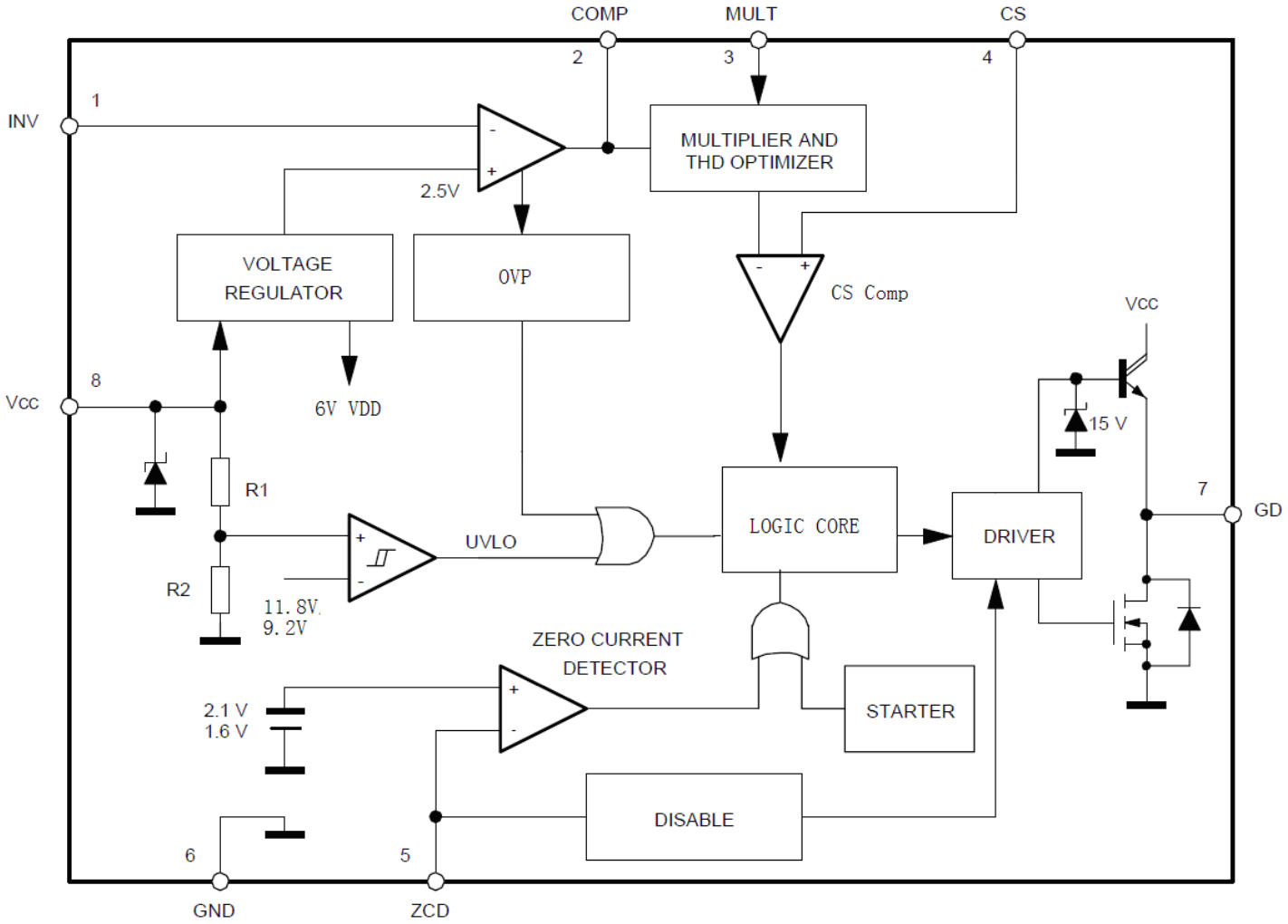
Pin Num.	Symbol	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV pin to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high VCC.
8	VCC	Supply Voltage.

Absolute Maximum Ratings

Parameter	Value	Unit
Voltage at VDD pin to GND:VDD	-0.3～30	V
Voltage at CS,INV,MULT,COMP PIN to GND	-0.3～8	V
Output Totem Pole Peak Current: IGD	±0.8	A
Zero Current Detector Max. Current	-50（source） 10(sink)	mA
Min/Max operating Junction Temperature T_J	-40～150	°C
Lead Temperature (Soldering, 10secs)	260	°C
Min/Max Soldering temperature Tskj	-55～150	°C

Caution: The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

Block Diagram



Electrical Characteristics

（T_A =25 °C, V_{CC} =12V,Co=1nF, unless otherwise noted.）

Item	Symbol	Test condition	Min	Typ.	Max	Unit
Supply Voltage(VDD) section						
VCC	Operating range	After turn-on	10.5		21	V
VCCon	Turn-on threshold	(1)	10.5	11.8	13	V
VCCOff	Turn-off threshold	(1)	8.4	9.2	10	V
Hys	Hysteresis		2.2		2.8	V
V_Z	Zener Voltage	I_{CC} = 20 mA	21	23	26	V
Current sense input section						
$I_{start-up}$	Start-up Current	Before turn-on, V_{CC} =11V		110	120	μA
Iq	Quiescent Current	After turn-on		1.5	2.0	mA
I_{CC}	Operating Supply Current	Vcc=15V		1.8	2.5	mA
Multiplier input section						
I_{MULT}	Input Bias Current	V_{VFF} = 0 to 4 V			-1	μA
V_{MULT}	Linear Operation Range		0 to 3			V
$\frac{\Delta V_{CS}}{\Delta V_{MULT}}$	Output Max. Slope	V_{MULT} = 0 to 0.5V V_{COMP} = Upper clamp	1.65	1.9		V/V
K	Gain (2)	V_{MULT} = 1 V, V_{COMP} = 4 V	0.5	0.6	0.7	1/V
Error amplifier section						
V_{INV}	Voltage Feedback Input Threshold	10.5V<V_{CC}<22V	2.475	2.5	2.525	V
	Line Regulation	V_{CC}=10.5 to 22V		2	5	mV
I_{INV}	Input Bias Current	V_{INV} = 0 to 3 V			-1	μA
G_V	Voltage Gain	Open loop	60	80		dB
GB	Gain-Bandwidth Product			1		MHz
I_{COMP}	Source Current	V_{COMP} = 4V, V_{INV} = 2.4 V	-2	-3.5	-5	mA
	Sink Current	V_{COMP} = 4V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper Clamp Voltage	I_{SOURCE} = 0.5 mA	5.3	5.7	6	V
	Lower Clamp Voltage	I_{SINK} = 0.5 mA(1)	2.1	2.25	2.4	V
Current sense comparator section						
I_{CS}	Input Bias Current	V_{CS} = 0			-1	μA
td(H-L)	Delay to Output			200	350	ns
$V_{CS\ clamp}$	Current sense reference clamp	V_{COMP} = Upper clamp	1.6	1.7	1.8	V
$V_{CSoffset}$	Current sense offset	V_{MULT} = 0		30		mV
		V_{MULT} = 2.5V		5		

Zero current detector section						
V_{ZCDH}	Upper Clamp Voltage	I_{ZCD} = 2.5 mA	5.0	5.7	6.5	V
V_{ZCDL}	Lower Clamp Voltage	I_{ZCD} = -2.5 mA	0.3	0.65	1	V
V_{ZCDA}	Arming Voltage (positive-going edge)	(3)		2.1		V
V_{ZCDT}	Triggering Voltage (negative-going edge)	(3)		1.6		V
I_{ZCDb}	Input Bias Current	V_{ZCD}= 1 to 4.5 V		2		µA
I_{ZCDsrc}	Source Current Capability		-2.5		-5.5	mA
I_{ZCDsnk}	Sink Current Capability		2.5			mA
V_{ZCDdis}	Disable threshold		150	200	250	mV
V_{ZCDen}	Restart threshold				350	mV
I_{ZCDres}	Restart Current after Disable		30	75		µA
Starter						
t_{START}	Start Timer period		75	130	300	µs
Output overvoltage section						
I_{OVPH}	Dynamic OVP triggering current		36	40	44	µA
I_{OVPL}	Dynamic OVP release current		4	7	10	µA
Hys	Hysteresis	Hys= I_{OVPH}- I_{OVPL} (3)		30		µA
Gate driver						
V_{OH}	Dropout Voltage	$I_{GDsource}$ = 20 mA		2	2.6	
		$I_{GDsource}$ = 200 mA		2.5	3	V
V_{OL}		I_{GDsink} = 200 mA		0.9	1.9	V
tf	Voltage Fall Time			30	70	ns
tr	Voltage Rise Time			40	80	ns
V_{Oclamp}	Output clamp voltage	$I_{GDsource}$ = 5mA; Vcc = 20V	15	15.5	16	V

(1)All parameters are in tracking

(2)The multiplier output is given by: $V_{CS}=K*V_{MULT}*(V_{COMP}-2.5)$

(3)Parameters guaranteed by design, functionality tested in production.

Operation Description

● **Overvoltage protection**

Under steady-state conditions, the voltage control loop keeps the output voltage Vo of a PFC pre-regulator close to its nominal value, set by the resistors R1 and R2 of the output divider. Neglecting ripple components, the current through R1, I_{R1}, equals that through R2, I_{R2}. Considering that the non-inverting input of the error amplifier is internally referenced at 2.5V, also the voltage at pin INV will be 2.5V, then:

$$I_{R2}=\frac{2.5}{R2}=I_{R1}=\frac{V_O-2.5}{R1}$$

If the output voltage experiences an abrupt change ΔVo > 0 due to a load drop, the voltage at pin INV will be kept at 2.5V by the local feedback of the error amplifier, a network connected between pins INV and COMP that introduces a long time constant to achieve high PF (this is why ΔVo can be large). As a result, the current through R2 will remain equal to 2.5/R2 but that through R1 will become:

$$I'_{R1} = \frac{V_O - 2.5 + \Delta V_O}{R1}$$

The difference current ΔIR1=I'R1-IR2=I'R1-IR1=ΔVo/R1 will flow through the compensation network and enter the error amplifier output (pin COMP). This current is monitored inside the ME8401 and if it reaches about 37 μA the output voltage of the multiplier is forced to decrease, thus smoothly reducing the energy delivered to the output. As the current exceeds 40 μA, the OVP is triggered (Dynamic OVP): the gate-drive is forced low to switch off the external power transistor and the IC put in an idle state. This condition is maintained until the current falls below approximately 10 μA, which re-enables the internal starter and allows switching to restart. The output ΔVo that is able to trigger the Dynamic OVP function is then:

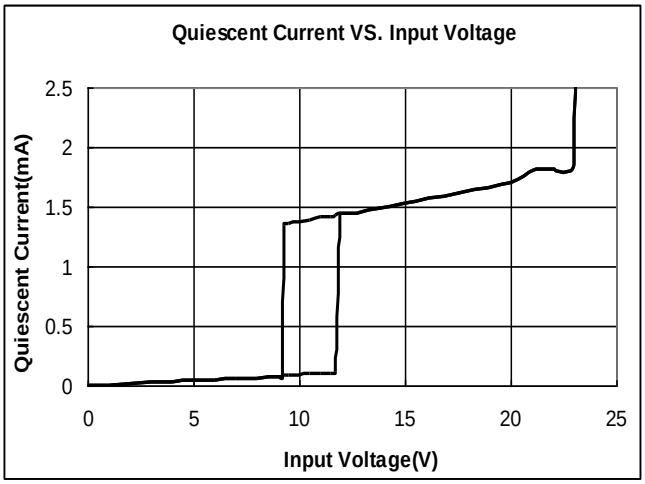
$$\Delta V_O = R1 \cdot 40 \cdot 10^{-6}$$

An important advantage of this technique is that the OV level can be set independently of the regulated output voltage: the latter depends on the ratio of R1 to R2, the former on the individual value of R1. Another advantage is the precision: the tolerance of the detection current is 12%, that is 12% tolerance on ΔVo. Since ΔVo << Vo, the tolerance on the absolute value will be proportionally reduced. Example: Vo = 400V, ΔVo = 40V. Then: R1=40V/40uA=1MΩ; R2=1MΩ·2.5/(400-2.5)=6.289KΩ. The tolerance on the OVP level due to the ME8401 will be 40*0.12=4.8V, that is 1.2% of the regulated value.

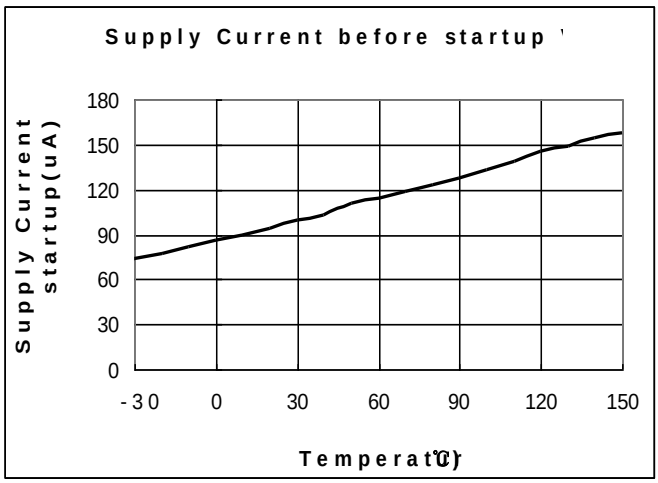
When the load of a PFC pre-regulator is very low, the output voltage tends to stay steadily above the nominal value, which cannot be handled by the Dynamic OVP. If this occurs, however, the error amplifier output will saturate low; hence, when this is detected, the external power transistor is switched off and the IC put in an idle state (Static OVP). Normal operation is resumed as the error amplifier goes back into its linear region. As a result, the ME8401 will work in burst-mode, with a repetition rate that can be very low. When either OVP is activated the quiescent consumption of the IC is reduced to minimize the discharge of the Vcc capacitor and increase the hold-up capability of the IC supply system.

Typical performance characteristics

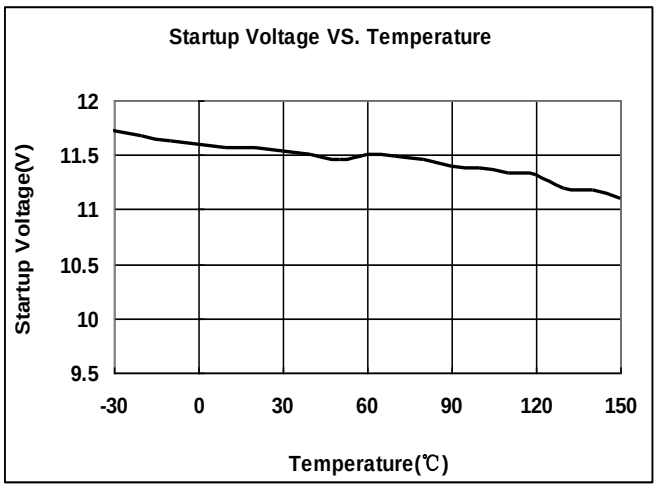
(1) IC Supply Current vs. Input Voltage



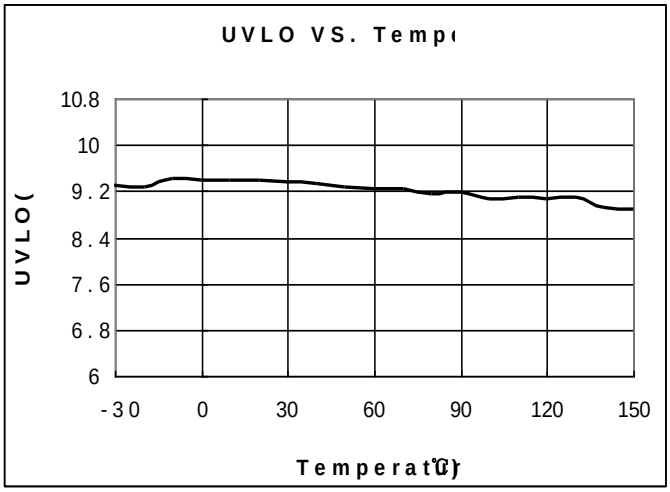
(2) Startup Current vs. Temperature



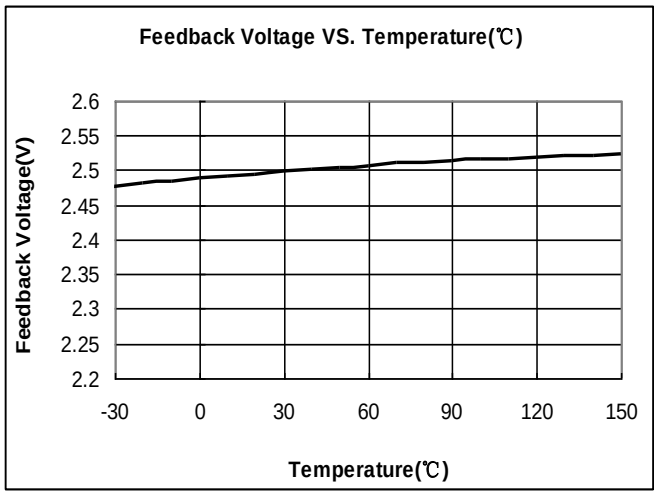
(3) VDD under voltage lock out exit voltage vs. Temperature



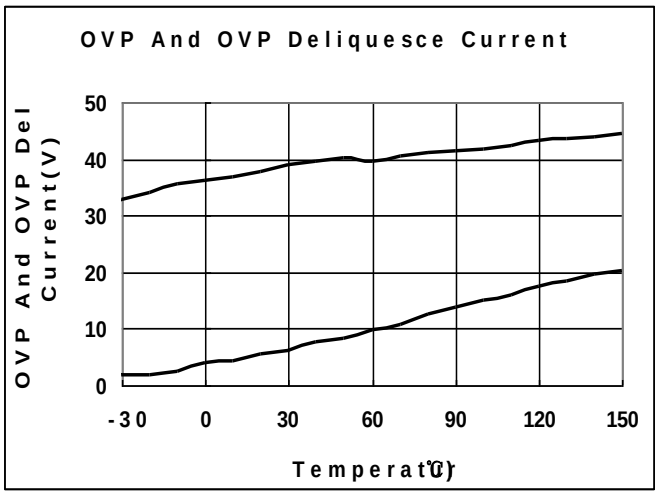
(4) VDD under voltage lock out enter voltage vs. Temperature



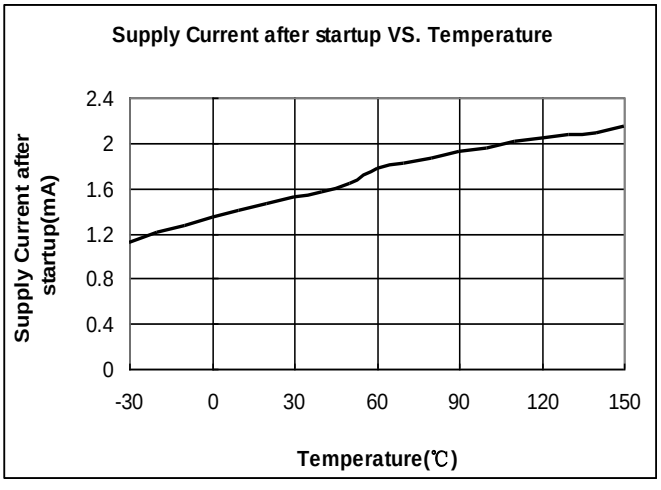
(5) Reference voltage for feedback vs. Temperature



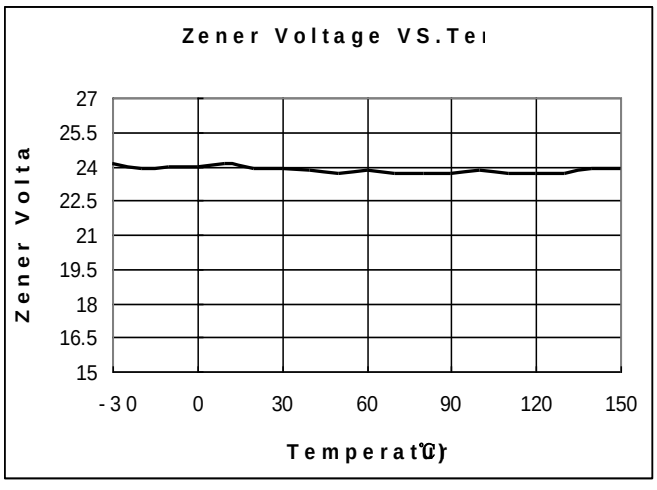
(6) OVP And OVP Deliquesce Current vs. Temperature



(7)Quiescent Current vs. Temperature

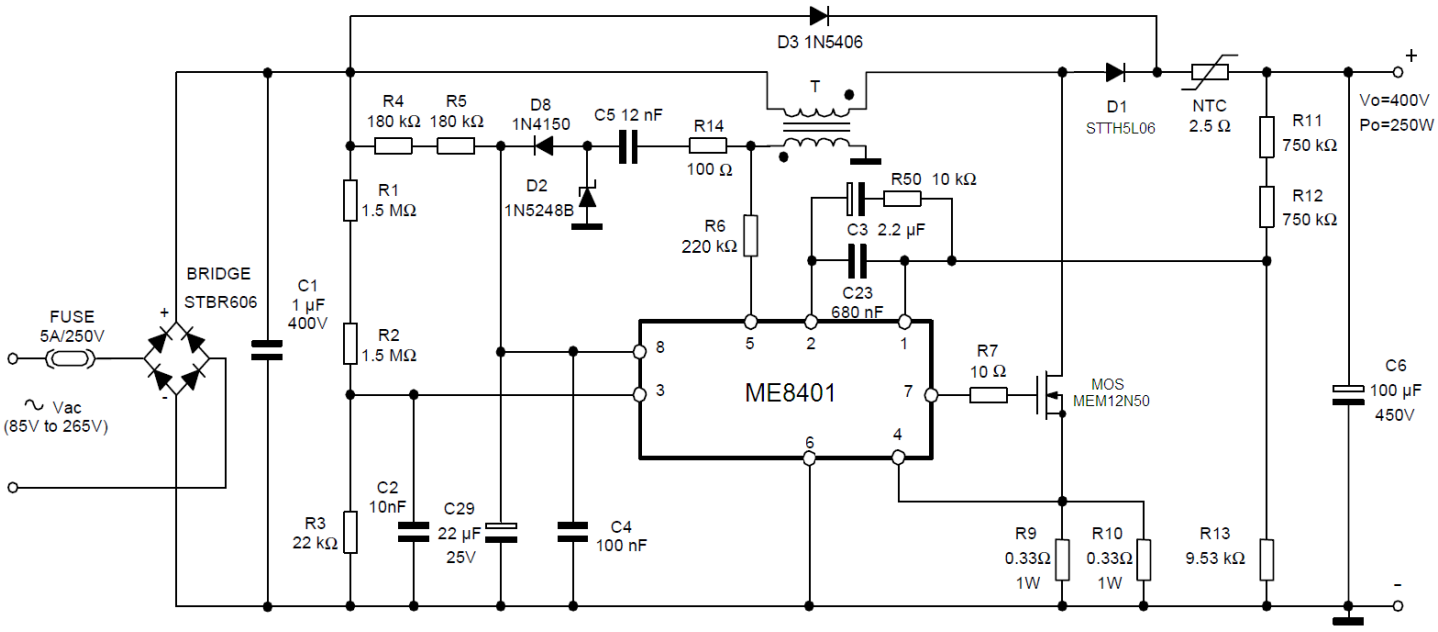


(8) Zener Voltage vs.Temperature

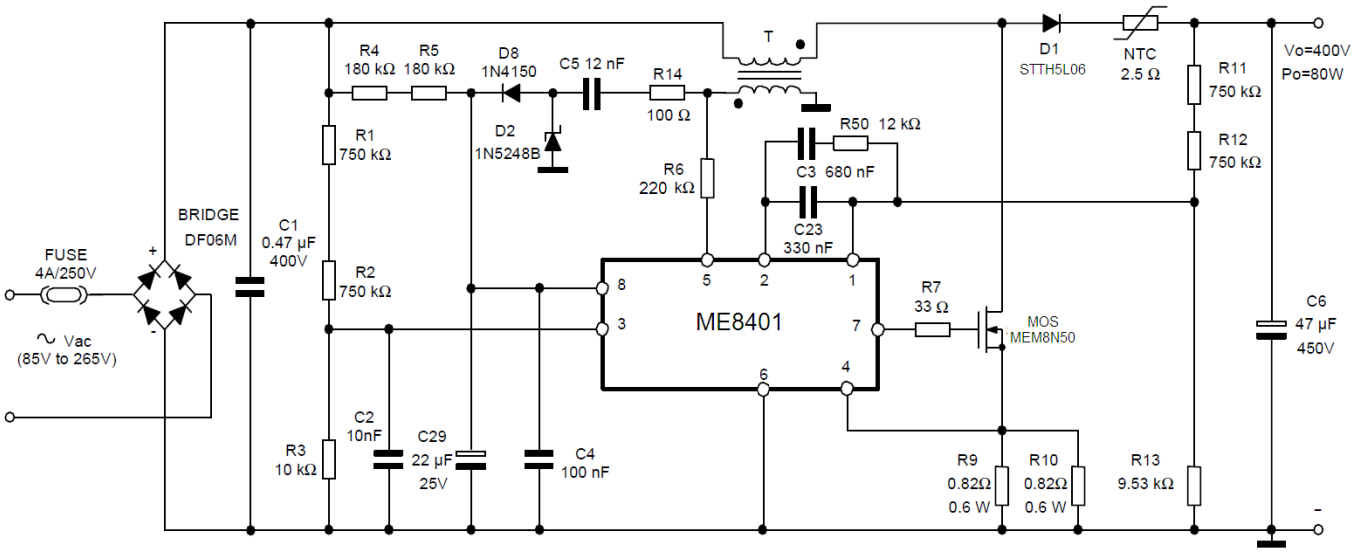


Typical Application

(1)Typical application circuit (250W, Wide-range mains)



(2)Typical application circuit (80W, Wide-range mains)

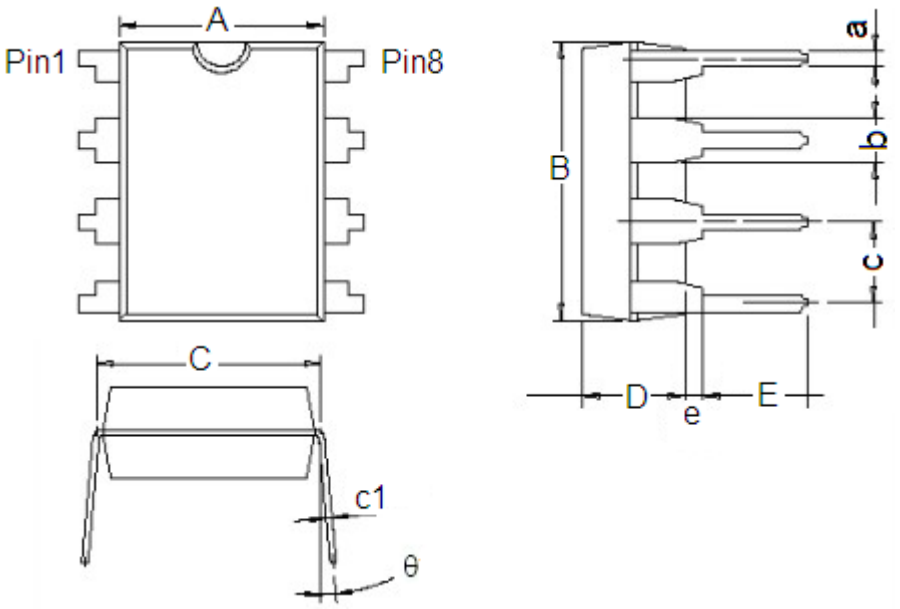


Boost Inductor Spec (ITACOIL E2543/E)

- E25x13x7 core, 3C85 ferrite
- 1.5 mm gap for 0.7 mH primary inductance
- Primary: 105 turns 20x0.1 mm
- Secondary: 11 turns 0.1 mm

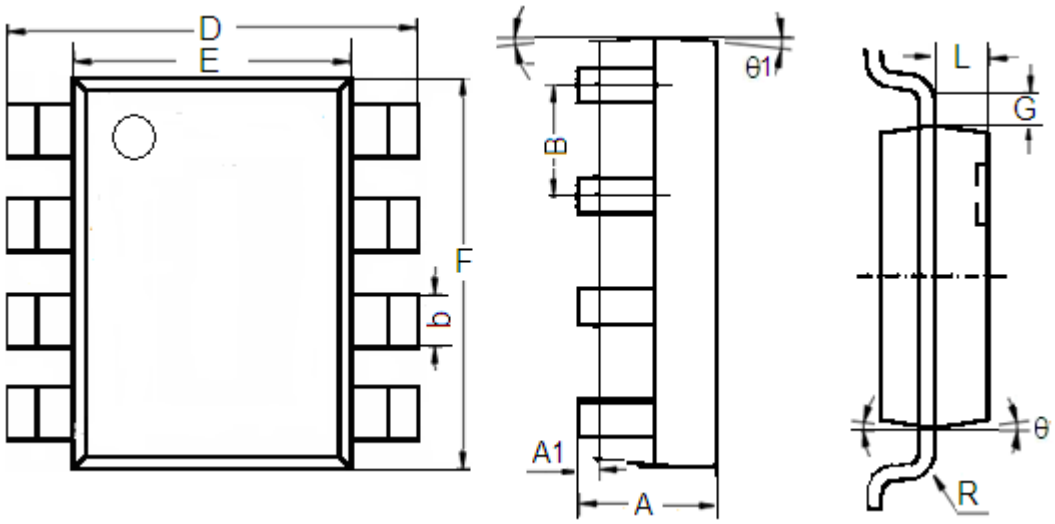
Package Information

Package type:DIP8 Unit:mm(inch)



Character	Dimension (mm)		Dimension (Inches)	
	Min	Max	Min	Max
A	6.200	6.600	0.244	0.260
B	9.000	9.400	0.354	0.370
C	7.620(Typ.)		0.300(Typ.)	
D	3.200	3.600	0.126	0.142
E	3.000	3.600	0.118	0.142
a	0.360	0.560	0.014	0.022
b	1.524(Typ.)		0.060(Typ.)	
c	2.54(Typ.)		0.100(Typ.)	
c1	0.204	0.360	0.008	0.014
e	0.510(Min)		0.020(Min)	
θ	0^0	15^0	0^0	150

Package type:SOP8 Unit:mm(inch)



Character	Dimension (mm)		Dimension (Inches)	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.1	0.3	0.004	0.012
B	1.27(Typ.)		0.05(Typ.)	
b	0.330	0.510	0.013	0.020
D	5.8	6.2	0.228	0.244
E	3.800	4.000	0.150	0.157
F	4.7	5.1	0.185	0.201
L	0.675	0.725	0.027	0.029
G	0.32(Typ.)		0.013(Typ.)	
R	0.15(Typ.)		0.006(Typ.)	
θ1	7°		7°	
θ	8°		8°	

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